REMARKS

Claims 1, 3 – 7, and 9 – 11 remain in the application and stand rejected. Claims 2 and 8 are canceled and claims 9 and 10 are amended herein. Claims 12 – 31 are canceled herein without prejudice as being drawn to a non-elected invention. New claims 32 – 51 are added herein. The rejection of claims 1 – 11 is respectfully traversed.

New claims 32 – 51 are supported by the specification as filed and by canceled claims 12 – 31. No new matter is added.

Claims 1 – 4 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. patent No. 6,567,763 to Javanifard et al. The applicants note that claim 5 is not rejected and so, is deemed to be allowable, but objected to for depending from a rejected base claim. Claims 6 – 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Javanifard et al. in view of U.S. patent No. 6,496,056 to Shoji. Claims 9 – 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. patent No. 6,008,685 to Kunst in view of Shoji. The rejection is respectfully traversed.

Claim 1 has been amended to include the recitations of claim 2, and so, is claim 2 rewritten in independent form. No new matter has been added.

In rejecting claim 2 it is asserted that Javanifard et al. device comprises "switches (clamp) for selectively **shunting** current from the constant current source." (emphasis added). The Javanifard et al. switches are not clamps within the ordinary meaning used in the art. Javanifard et al. Figure 2 shows switches S225 and S235 in series with constant current sources A230 and A240, respectively. Therefore, while opening switch S225 or S235 may block current flow from either of constant current sources A230 or

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A240, closing either of the switches S225 and S235 does not shunt current from either supply A230 or A240. Instead, Javanifard et al. teaches that

> Switches 225, 235, and 245 are controlled so that currents 231 and 241 are sequentially applied to diode 210. At a first instant in time, switch 225 is closed, switch 235 is open, and switch 245 is coupled to node 246. In which case, the voltage at diode 210 due to current 231 is stored in analog register 250.

Col. 4, line 63 – col. 5, line 1. None of this describes any of the switches 225, 235 or 245 shunting current from any of the Javanifard et al. constant current sources A230 or A240. Neither is such a modification of suggested. Therefore, neither Javanifard et al. nor any reference of record teaches or suggests "a switchable current source" with "a clamping device selectively shunting current from said constant current source" as recited by claim 1 as amended. New claims 38 and 47 include analogous recitations. Further, new claim 47 specifically recites that the clamping device is in parallel with the constant current source, which the references of record also fail to teach or suggest. *See also*, claims 37 and 46. Accordingly, Javanifard et al. does not teach the present invention as recited in claim 1 as amended or in new claims 37, 38, 46 and 47.

Furthermore, since dependent claims include all of the differences with the references as the claims from which they depend, the present invention as recited in claims 3 and 4, which depend from claim 1, is patentable over Javanifard et al. Reconsideration and withdrawal of the rejection of claims 1, 3 and 4 under 35 U.S.C. §102(b) is respectfully requested.

Regarding the rejection of claims 6 – 8 over the combination of Javanifard et al. with Shoji, Shoji teaches

> A voltage regulator generates a reference voltage which is determined at least in part based on known process parameter variations in the ring oscillator. The ring oscillator utilizes the reference voltage generated by the voltage regulator as its power supply voltage, and its oscillation period is thereby made insensitive to the process parameter variations. In addition, back-bias effects may be introduced in the voltage regulator to

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> compensate back-bias effects resulting from particular configurations of the ring oscillator.

Col. 2, lines 20 – 23. See, also, Figures 2 and 3. While Shoji does show PFETs and NFETs connected into circuits including ring oscillators, as far as the applicants can tell, Shoji does not teach or suggest "a clamping device selectively shunting current from said constant current source" as either of canceled claim 8 and amended claim 1 recite. Neither does Shoji teach selectively providing current to a PN junction that "is a FET body to source/drain junction" as recited in claim 6. This is described in the specification on page 5, lines 10 – 29 with reference to Figure 1. The applicants note that this involves forward biasing the source/drain junction, which is far from a usual CMOS circuit application. Nor does Shoji teach selectively providing current to the body of a FET at a source/drain junction in a CMOS IC as recited in claim 7. Accordingly, the combination of Shoji with Javanifard et al. does not result in the present invention as recited in claim 1, much less claims 6 and 7 which depend therefrom.

Regarding the rejection of claims 9 – 11 over the combination of Kunst with Shoji, it is asserted that "Kunst teaches the device as stated above." Applicants note that this is the first mention of Kunst and nothing specific is indicated with respect to application of Kunst. Be that as it may, Applicants further note that Kunst shows a number of current supplies I_1, I_2, ... I_M, each series connected with a switch S_1, S_2, ... S_M. However, Kunst also fails to teach or suggest "a clamping device selectively shunting current from said constant current source" as either of canceled claim 8 and amended claim 1 recite. Regarding Shoji, it is asserted that "Shoji discloses in Fig. 2-5 and col. 3 a device including all deficient limitations of claims 9-11." However, as noted hereinabove, Shoji fails to teach the recitations of claims 6 and 7 from which claims 9 – 11 depend. Therefore, for the reasons that Shoji fails to provide what is missing from Javanifard et al. to result in the present invention as recited in claims 1, 6 and 7, Shoji in combination with Kunst fails to result in the present invention as recited in claims 9 – 11. Reconsideration and withdrawal of the rejection of claims 6, 7 and 9 – 11 under 35 U.S.C. §103(a) over is respectfully requested.

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Furthermore, regarding new claims 32 – 51, in addition to the differences noted above with respect to independent claims 37, 38, 46 and 47, no reference of record teaches or suggests that the PN junction is a CMOS inverter (claims 32, 43 and 47) in a ring oscillator (claims 33, 44 and 47), that may include a NAND gate gated by the switch selection (claims 34, 45, 46 and 48, 49). Accordingly, new claims 32 – 51 are believed to be allowable over all references of record. Independent consideration and allowance of new claims 32 – 51 over is respectfully requested.

The applicants have reviewed the references cited, but not relied upon in the rejection and find them to be no more relevant than the reference upon which the rejection is based.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance, both for the amendment to the claims and for the reasons set forth above, the applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 1, 3 – 7 and 9 – 11 under 35 U.S.C. §§102(b) and 103(a), consider new claims 31 – 52 and allow the application to issue.

The applicants note that MPEP §706 "Rejection of Claims," subsection III, "PATENTABLE SUBJECT MATTER DISCLOSED BUT NOT CLAIMED" provides in pertinent part that

> If **the examiner** is satisfied after the search has been completed that patentable subject matter has been disclosed and the record indicates that the applicant intends to claim such subject matter, he or she **may note** in the Office action that **certain aspects or features** of the patentable invention have not been claimed and that if properly claimed such claims **may be given favorable consideration**. (emphasis added.)

The applicants believe that the written description of the present application is quite different than, and not suggested by, any reference of record. Accordingly, should the Examiner believe anything further may be required, the Examiner is requested to contact

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the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,

April 12, 2006
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